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A Novel Approach to Control Leakage Power in CMOS Circuits

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Abstract

In Present days, leakage power dissipation has become most dominant factor in low power VLSI designs, depends on moores law. When we want to decrease the threshold voltage which makes to increasing in subthreshold leakage current, so that leakage power dissipation becomes very high. According to International Technology Roadmap for Semiconductors (ITRS), total power dissipation which is effected by leakage power dissipation [1]. Due to the leakage power dissipation, All the electronic gadjects which are operated on the battery should drained fast, When the battery is in standby mode. In nano technology based devices, leakage power dissipation plays a major role. In this paper we present past different design approaches to reduce leakage power dissipation along with the proposed LECTOR (lekage control transistors) approach, which is an effective model to reduce leakge power dissipation. It is verified by the present literature to leakage power minimization approach for a specific application can be effectively carried by a VLSI circuit designer based on sequential analytical approach.

Keywords:

Subthreshold leakage current;

Leakage power dissipation,;

Submicron technology;

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1. Introduction:

Depending on the Moore's law, the transitor count on the chip be doubled per every two years. That means the technology is also changes from micron technology to submicron technology and it to deep submicron technology and finally it is to nano technology, which is depends on the shrinking on the feature size of the transistor. through the several complicated process is enabled planned to integrated on a single chip. In Present days all the electronic gadjects and systems are battery and powerd systems. So we want to increase the battery life. Generally all the portable devices such as notepads, personal computers, mobile phones, ipod's, and all hearing aids will have very low power requirements.When the lasting of battery is long, then the device makes better.The power dissipation has not made smaller even though with the scaling down of the supply voltage. The issue of heat removal and power dissipation is get worse as the magnitude of power per unit area has fulfill the growing. For the reason of increasing power consumption of present day chips, they invent cooling devices. The cost associated with the packaging and the cooling of such devices has more costly. In addition to cost, the issue of reliability is also a major concern. For every 10^0C increase in temperature makes component failure rate doubles. By minimizing the power consumption has became currently an extremely challenging area of research.

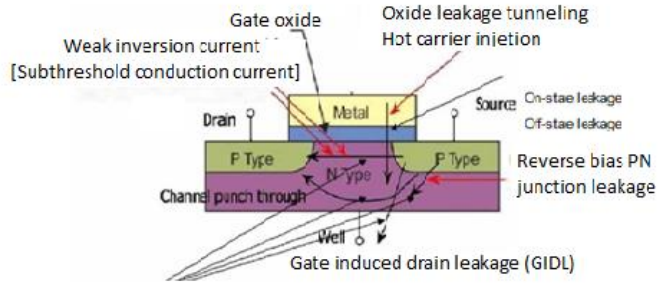


Fig.1 General CMOS leakage sources

Generally Leakage power (static) of a CMOS transistor depends on gate length and oxide thickness [2]. When we want performance degeneration then we decrease the supply voltage. When we want to scale down the threshold voltage along with the supply voltage, leads to speed up the device which results in exponential increase in the sub-threshold leakage current, thereby increase in the lekage power dissipation. Figure 1 shows that the major leakage sources of CMOS transistor. When the transistor is in OFF state, then reverse current flow (Sub threshold leakage power) occurs through in the circuit, which leads to leakge current. When we shrink the feature size of transistor, then automatically channel length decreases, there after increasing the leakage power in the total power dissipated as shown in Figure 1.1. Hence this leakage power which is gradually increases by 32 times in near future [3]. In present CMOS based leakage currents are Reverse-biased junction leakage current, Gate induced drain leakage, Gate direct-tunnelling leakage and Subthreshold (weak inversion) leakage current. Among those leakage currents subthreshold leakage current is most important challenge for research in present and future silicon based technologies.

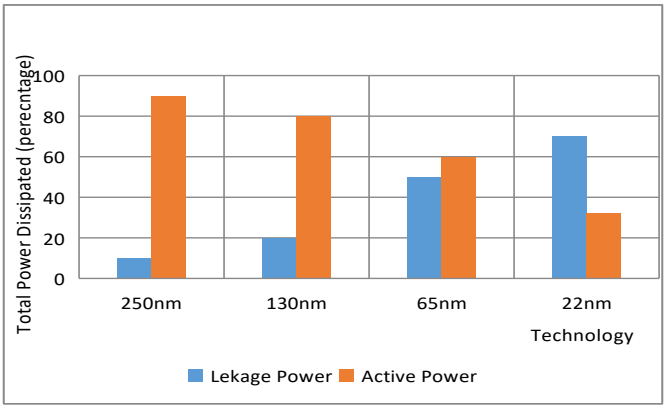


Fig.1.1 Total power dissipation

2. Previous Methods:

A.BASE APPROACH::

Base approach is a traditional approach, which we have a conventional CMOS transistor. In this approach is also called as an CMOS inverter. In this base case approach we have pull and puyll down networks. For pull up network we are using as PMOS transistors and for pull down network we are using NMOS transistor. Because of Logic high is good for PMOS and logic low is good for NMOS trasnsitors. The circuit operation of conventional CMOS is, when we apply low input compared to threshold voltage (Vgs < Vth) after some time PMOS transistor will turns ON. And NMOS transistor will turns OFF. Where as when we apply high input compared to threshold voltage (Vgs > Vth) then at some time PMOS transistor will turns OFF and NMOS transistors will turns ON.

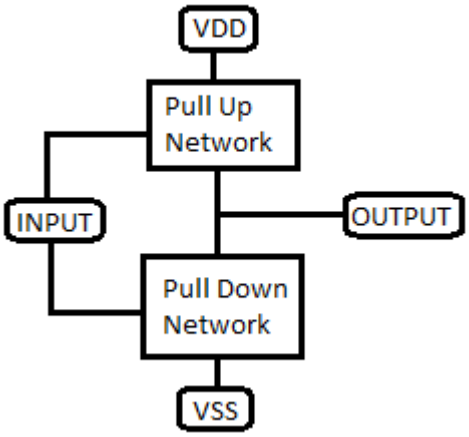


Fig.2.1 Sleep transistors with conventional CMOS

The total power dissipation which is the combination of Static power dissipation, Dynamic power dissipation and Short circuit power Static power dissipation. These leakage currents are occurs because of transistors leakage currents, when either PMOS or NMOS transsitor is OFF at every time simentaniously.
Expression for Static Power dissipation (leakage power) :-

$$\textbf{Power (P)} = V_{DD} * \textbf{leakage current}$$

Expression for Static Power dissipation :- This Dynamic power dissipation takes place due to the charging and discharging of capacitor .

$$P = ACV^2F$$

Where, P is the power consumed, A is the activity factor, i.e., the fraction of the circuit that is switching, C is switched capacitance, V is supply voltage and F is the clock frequency.

B. SLEEP TRANSISTOR APPROACH:

In this approach, we want to sleep the transistor.That means when the transistor is in OFF state only we get leakage current. when we want to sleep that OFF transistor then automatically we control leakage current. For the sleeping of pull and and pull down networks, we add another High Vth of PMOS which is in between vdd and pull up network. And another High Vth of NMOS is in between Pull down network to ground. This approach is also called as the MTCMOS (Multi Threshold CMOS). It is shown in Figure 2.2.

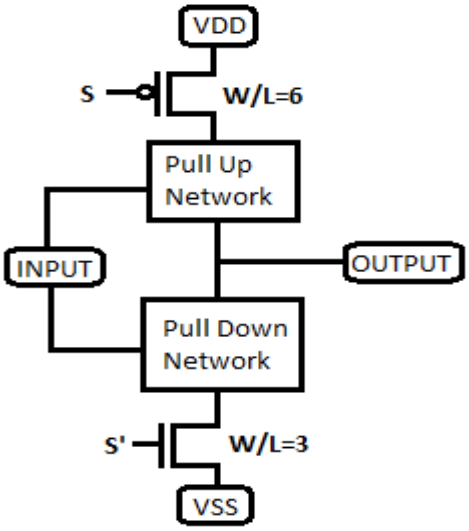


Fig.2.2 Sleep transistors with conventional CMOS

Here, The sleep transistors S and S' are turned off when the logic circuits are not in use. By using this approach it gradually reduces leakage power when the circuit is in sleep mode. If we further increasing the sleep transistors which is leads to increases circuits area and delay. Furthermore, the pull-up and pull-down networks will have floating values and thus will lose state during sleep mode. These floating values will have an impact on wakeup time and energy of the sleep approach due to the requirement to recharge transistors which lost state during sleep.

C. FORCED STACK APPROACH:

Another approach to reduce leakage power is to stack the transistors. Here stacking means we want to split the transistors into two by its scalling. Stacking the transistors result to reduce subthreshold lekage current. Shown in fig. 2.3

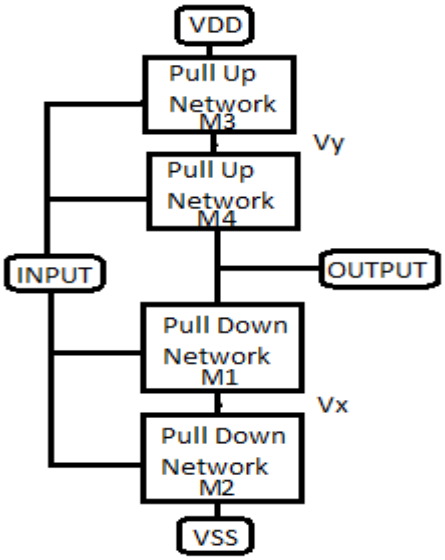


Fig.2.3 Forced stack CMOS Approach

The stacking effect can be understood from the forced stack inverter[4] shown in figure 2.3. In the general inverter there are only one NMOS and one PMOS transiostor. But here in forced stack appraoch we used two pull up transistors and two pull down transistors. In this approach we have the only one input which is shared

to all the transistors. Suppose when we apply input is as '0', then both pull down transistor M1 and M2 are turned off. And Vx is the central node voltage.Transistor M2 has its internal resistance. Then the resistance Vx is greater than the ground potential.This positive Vx results in a negative gate-source (Vgs) for the Ml transistor and the negative source-base voltage (Vsb) for Ml. Here Ml also has a reduced drain-source voltage (Vds), which lower the Drain induced barrier lowering (DIBL) effect.

These three effects together reduced the factor X in equation and hence the leakage power. All transistors are getting the same input. So this forced stack technique is a state saving technique. That means when the circuit is in OFF mode it saves the current state. The main drawback of this forced stack inverter is that it can not use the high Vth transistor. Because if it use the high Vth transistor than there is a dramatic increase of delay. This delay increase is 5X larger than the conventional CMOS.

D. SLEEP STACK APPROACH:

Sleepy stack approach is the combination of forced stack and the sleep transistor techniques [5]. Hence the names comes as sleepy stack. The sleepy stack inverter is shown in figure 2.4. It uses the aspect ratio W/L = 3 for the pull up transistors and W/L =1.5 for the pull down transistors. At the same time the conventional inverter with the same input capacitance uses the aspect ratio W/L = 6 for the pull up transistors and W/L = 3 for the pull down transistors.

Here = 2^p is assumed. In the previous approaches sleep transistor and the stacked transistors are in parallel connections. But in this sleep stack approach the width of the sleep transistors is reduced. By Changing the width of the sleep transistors may provide additional trade offs between the factors of power, area and delay. Sleep transistors work in the sleep stack is same as the activity of the sleep transistors in the sleep transistor technique. The general process of sleep transistor are during in active mode the sleep transistors are turned on while during sleep mode the sleep transistors are turned off. Here this sleepy stack approach can reduce the circuit delay in two ways. First, during active mode the sleep transistors are always on so there is always a current flow through the circuit.

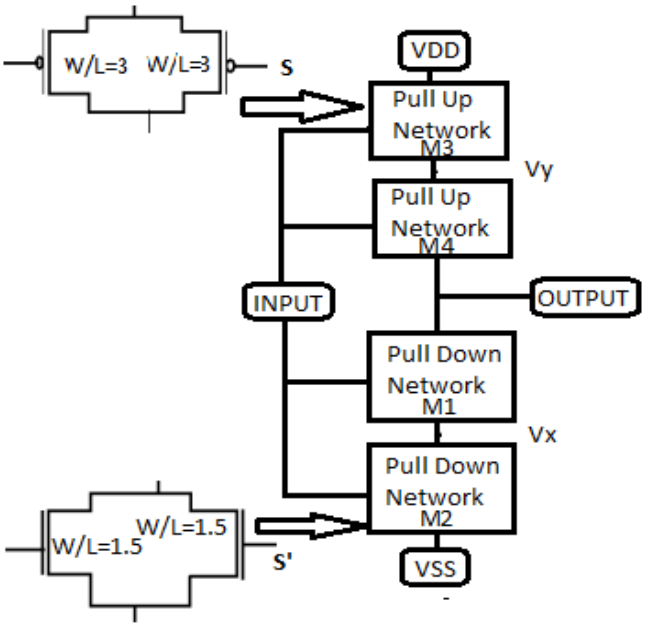


Fig.2.4 Forced stack with conventional CMOS

For that reason it gives a faster switching time than the forced stack structure. The high threshold voltage Vth transistors are used for the sleep transistor and the transistors parallel to the sleep transistor without producing large delay. In sleep mode operation both the sleep transistors are turned off. But in the sleepy stack approach

maintains exact logic state. As we used high threshold voltage Vth transistor here so the leakage power is suppressed. And stacked transistors are also reduced the leakage power consumption. So sleepy stack approach gets very low leakage power consumption during sleep mode while increasing area a lot.

E. SLEEPY KEEPER APPROACH:

In this Sleepy keeper approach it uses the traditional sleep transistors with two additional transistors which are totally the opposite type transistor to save state during in the sleep mode. To reduce the subthreshold leakge current we use multi threshold or dual threshold voltages. In the conventional CMOS design the NMOS are placed always at the pull down network because it is well known that NMOS transistors are not efficient at passing Vdd [6] shown in Figure 2.5. On the other hand PMOS transistors are placed at the pull up network because PMOS transistors are not efficient at passing GND.

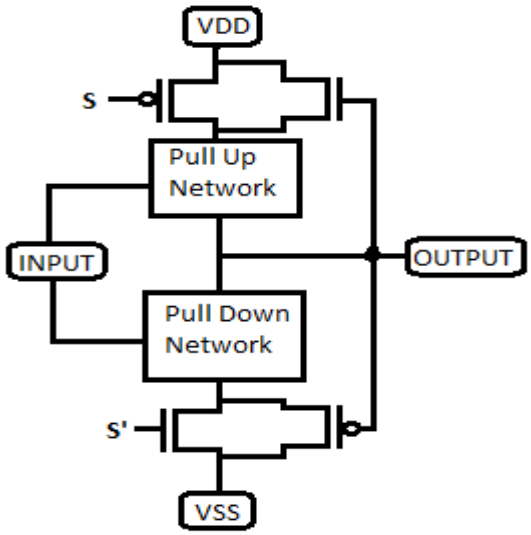


Fig.2.5 Sleepy keeper with conventional CMOS

Let the value of '1' is applied to sleep mode and assume that the value has already been calculated. The sleepy keeper [9] circuit in figure 3.1 uses this output value of '1' and an NMOS transistor maintains this value during sleep mode. An additional NMOS transistor is added in parallel to the pull up sleep transistor connected to VDD. At sleep mode this NMOS transistor is the only source of VDD to the pull-up network since the sleep transistor is off. Similarly, when we maintain a '0' value, assume that the value is already calculated. The sleepy keeper approach uses this output value of '0' and a PMOS transistor maintains the value during sleep mode. An additional PMOS transistor is added in parallel to the pull down sleep transistor connected to GND.

At sleep mode this PMOS transistor is only source of GND the pull down network since the sleep transistor is off. Sleep NMOS and sleep PMOS transistors were turned off during measurement of sub threshold leakage power dissipation in standby mode while for its measurement in active mode, all sleep NMOS and PMOS transistors were turned on.

3. Proposed Approach:

Leakage Control Transistor (LECTOR) :

Leakage Control Transistor is an approach to reduce the leakage problem in CMOS circuits. In this approach we have two additional leakage control transistors, named as self-controlled, in a path from supply to ground. This provides the additional resistance thereby reducing the leakage current in the path [7]. The main prons as compared to other approaches is, it involves the sleep transistor is that LECTOR Approach does

not have any other additional control circuitry. In active state this will limits the area increasing and also the power dissipation. Another main advantage of this leakage control transistor (LECTOR) approach is that it does not effect the dynamic power dissipation which is the major limitation with the other leakage reduction approachs.In this stacking technique the transitors path from supply rails to ground is the basic idea behind the LECTOR technique for the leakage power reduction. This approach is based on the previous approaches and leakage power from [1], [2] and [5]. Here in this state which have less leakage for more than one OFF transistor in a path from vdd to ground. The below Fig.3 shows the number of OFF transistors is related to leakage power.

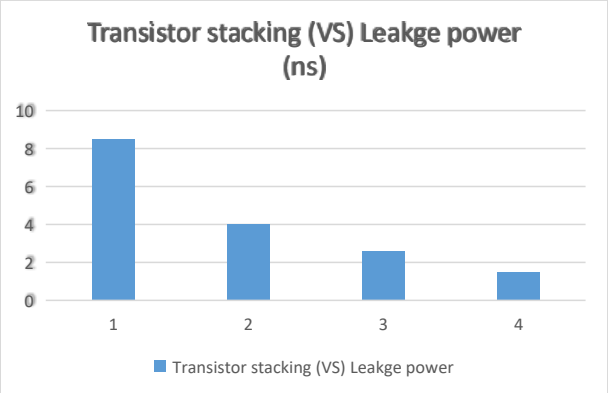


Fig.3 Number of OFF transistors is related to leakage power

In this approach two leakage control transistors are added between pull-up and pull-down network in the logic gate (one PMOS for pull-up and one NMOS for pull-down) for which the gate terminal of every Leakage Control Transistor (T1, T2) is controlled by the source of the other.This method ensures that among the T1 and T2s always operates in its close to cutoff region.

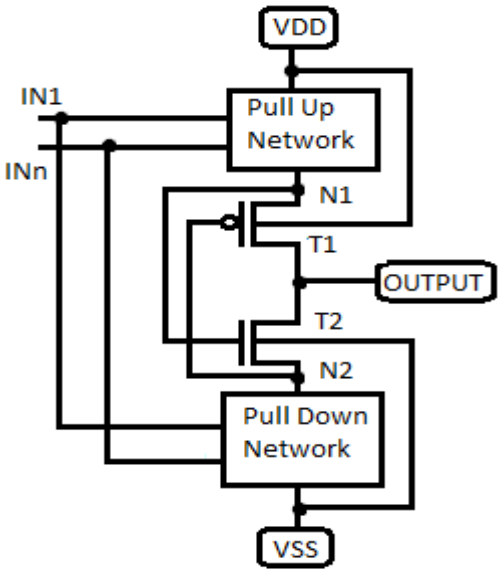


Fig.3.1 Number of OFF transistors is related to leakage power

This approach of a Lekage Control Transistors (LECTOR) CMOS gate is shown in Figure 3.1. Two LECTOR transistors's join between nodes N1 and N2. The gate terminal of every Lector transistor is controlled by the source of the other, hence it named as self-controlled stacked transistors. As This lekage control tranwistors are self-controlled, which doesn't requires external circuit is needed through the limitation using the sleep transistor technique has been triumph over. The introduction of T1 and T2s increases the resistance of the path

from Vdd to Gnd, therefore reducing the leakage current. Leakage Control Transistor (LECTOR) approach is verified in the case of an inverter. A LECTOR INVERTER is shown in Figure 3.2.

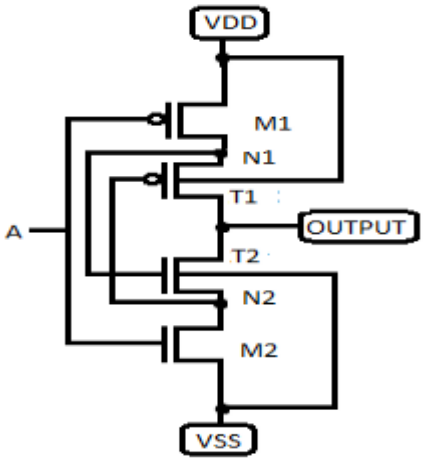


Fig.3.2 LECTOR basedinverter

A PMOS show as T1 and also a NMOS as T2 in the midst of N1 and N2 nodes of inverter. The output of inverter is taken from the connected drain nodes T1 and T2. The source nodes of T1 and T2 are the nodes N1 and N2 respectively of the pull-up and the pull-down logic. The gates of T1 and T2 are controlled by the potential at source terminal of T2 and T1 respectively. This connection at all times keeps one of the two Ts in its near cutoff region for any input.

When Vdd = 1V, input A = low, the voltage on the node N2 is 800 mV. And hence T1 can't be totally turned OFF because the voltage isn't sufficient. Hence the T1 resistance will be slightly lesser than it's OFF transistors resistance allowing conduction. The resistance provided by T1, even if it is not equal to the OFF resistance, increases the resistance within the path of VDD to ground, then it reducing the sub-threshold leakage current, attaining reduction in leakage power. Similarly, when input A = High, the voltage on the node N1 is 200 mV; so T2 would be operated in near cutoff state. The transistor M1 and M2 and also LECTOR based transistors T1 and T2 with all input vector A=0 & 1 Possibilities shown in table I.

Transistor name	Input vector (A=0)	Input vector (A=1)
M1	ON state	OFF state
M2	OFF state	ON state
T1	Near Cut-off state	ON state
T2	ON state	Near Cut-off state

Table I. LECTOR inverter possible inputs

Along using the resistance within the path, the propagation delay of the gate also gets increased. The LECTOR transistor inverter are sized which reduced propagation delay which is equal to conventional CMOS. In the all sleep related approach, the sleep transistors must be able to isolate the power supply and ground from the remaining of the transistors of the gate. Hence, they need to be very high dissipating & more dynamic power. This is occurs when the circuit is in idle state. Sleep transistor approach depends on input vector and it needs additional circuitry to monitor and control the switching of sleep transistors which consuming power in both active and idle states. While comparisation, LECTOR generates the required control signals within the gate and is also vector independent.

Two transistors are added in LECTOR approach in each and every path from Vdd to gnd regardless of number of transistors in pull-up and pull-down network. Where, forced stack approach have 100% area overhead. The loading condition with LCTs is a constant which is much lower. Where, the loading forced stacks approch depend upon number of transistors added. Hence, the performance degradation is insignificant when it comes to LECTOR approach, and we overcome the drawback faced by forced stack technique.

4. CMOS Logic gates using LECTOR Approach:

A.CMOS NAND GATE USING LECTOR:

The 2-input CMOS NAND gate is shown in Figure 4.1 with the two LCTs added to pull-up and pull-down network between the Vdd and gnd path. The simulation waveforms of LECTOR NAND show that the basic characteristics of NAND are retained by LECTOR NAND.

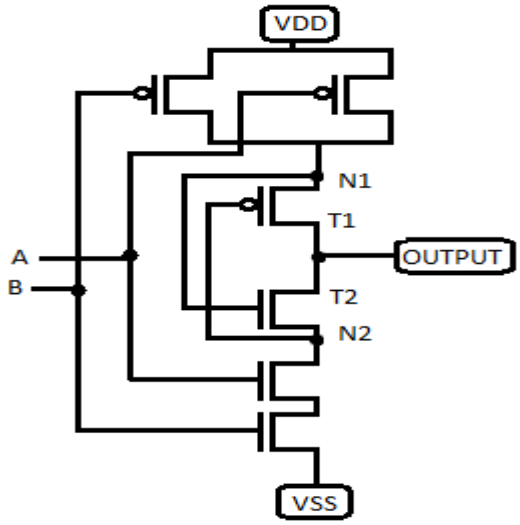
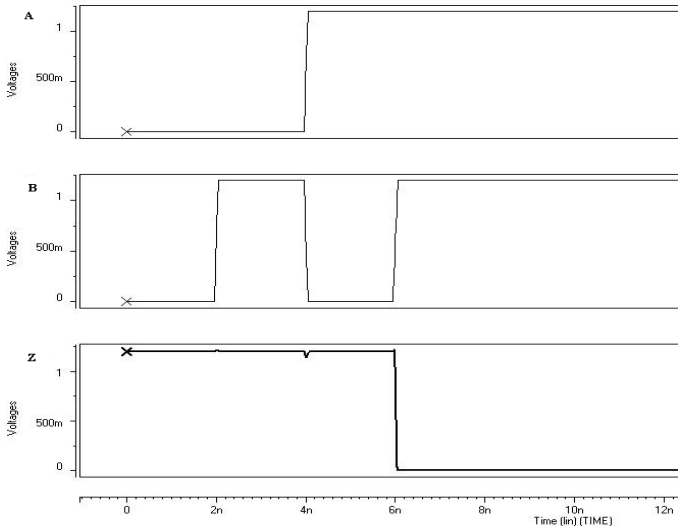


Fig.4.1 LECTOR based NAND gate

Output result of nand gate based LECTOR is shown in below



B. LECTOR BASED FULL ADDER :

The Gate level schematic of Full Adder is shownin Figure 4.2. The LECTOR implementation involves the addition of two LCTs for each gate. The transistor level schematic for full adder is same consists of LETOR transistor in between each gate.

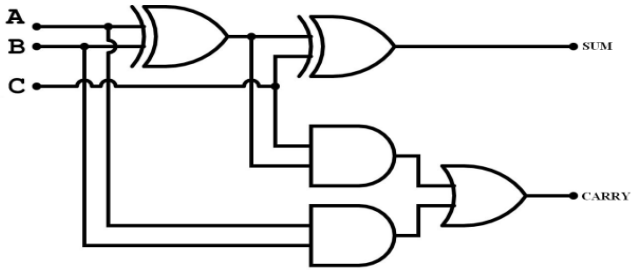
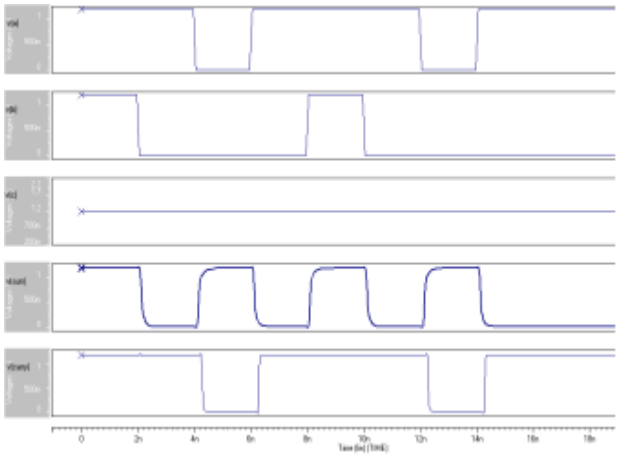


Fig.4.2 Gate level full adder

Here output shown in below for full adder in LECTOR model.



The simulation of all schematics is carried out by using Tanner EDA v15 tools. And verified with general conventional CMOS schematics.

V. EXPERIMENTAL RESULTS WITH TECHNOLOGY

Here this LECTOR based CMOS logic is verified with technology based verification. We considered 180nm, 90nm, 65nm and 45nm technology and compare those leakage power with the conventional cmos transistors technology files. The leakage power is measured using HSPICE simulator. If we want to consider the scaling down the technology, then supply voltage and threshold voltage values want to change it shown below.

Technology	180nm	90nm	65nm	45nm
Supply voltage	1.8v	1.2v	1.1v	1v
NMOS (Vt)	0.4	0.27	0.22	0.17
PMOS(Vt)	-0.42	-0.3	-0.22	-0.11

And also this technology scale down which is applied to LECTOR based design systems and compared with to its normal base case of cmos design.

❖ Conventional and LECTOR based Two input NAND gate leakage power:

Technology	Base case Leakage power (nA)	LECTOR Leakage power (nA)	decreasing leakage power
180nm	1.16	0.92	0.24
90nm	2.88	1.65	1.23
65nm	13.98	11.84	2.14
45nm	1503.6	1135	368.6

When the technology is scale down then automatically leakage power be decreases in LECTOR based system.

❖ Conventional and LECTOR based FULLADDER:

Technology	Base case Leakage power (nA)	LECTOR Leakage power (nA)	decreasing leakage power
90nm	42.38	24.25	18.13
45nm	92.44	54.24	38.2

Leakage power dissipation is taken as the average of power dissipations obtained at all the possible input vectors of the CMOS circuit. In general we have 4 possible combinations for 2-input NAND, hence the average of the four power dissipations gives the leakage power. In the case of full adder, the average of 8 power dissipations is considered to be as the static power dissipated. In each case, the leakage power is measured by exciting both the circuits (Conventional and LECTOR) with same set of input vectors.\

5. Conclusion:

As the technology is scale down into deep submicron to nano meter technology, it becomes a great challenge to tackle the problem of leakage power. LECTOR uses two transistors(T1,T2) that are controlled transistors. This Leakage control transistors achieves the reduction in leakage power which is ,more efficient compared to other approaches, such as sleepy stack, sleepy keeper, etc, along with the advantage of not affecting the dynamic power, since this technique does not require any additional control and monitor circuitry and also in this technique, the exact logic state is maintained. The LECTOR technique when applied to generic logic circuits in attaining up to 40-45% leakage reduction over the respective conventional circuits without affecting the dynamic power. A tradeoff between Propagation delay and area overhead exists here as the delay reduction by sizing the transistors will increase the area overhead.

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